Markov Models of Fault-Tolerant Memory Systems Under SEU

Luca Schiano, Marco Ottavi, Fabrizio Lombardi
Department of Electrical and Computer Engineering
Northeastern University
Boston, MA 02115, USA
{lschiano, mottavi, lombardi}@ece.neu.edu

Abstract

A Single Event Upset (SEU) can affect the correct operation of digital systems, such as memories and processors. This paper proposes novel Markov based models for analyzing the reliability and availability of different fault-tolerant memory arrangements under the operational scenario of an SEU. These arrangements exploit redundancy (either duplex or triplex replication) for dynamic fault-tolerant operation as provided by arbitration (for error detection and output selection) as well as in the presence of dedicated circuitry implementing different correction/detection codes for bit-flips as errors. The primary objective is to preserve either the correctness, or the fail-safe nature of the data output of the memory system for long mission time. It is shown that a duplex memory system encoded with error control codes has a higher reliability than the triplex arrangement. Moreover, the use of a code for single error correction and double error detection (SEC-DED) improves both availability and reliability compared to an error correction code with same error detection capabilities.

1. Introduction

Single high-energy particles (such as alpha particles and other ions [2]) can cause transient state changes (bit-flips) in both combinational circuits and memories of digital systems. Irradiating particles can cause ionization effects while transposing through a semiconductor material. If the variation in the charge of the affected area overcomes the noise threshold, then this can lead to a change of logic state, also called the Single Event Upset [11] (or SEU). For deep sub-micron technology, these phenomena are widely acknowledged to pose a significant threat to the correct operation of a system not only for space and avionic applications, but also at sea level [1, 5, 3].

Techniques to reduce the negative effects of SEUs have been proposed both at IC and system levels. At IC level, fault-avoidance techniques have been exploited through modifications and improvements in process technology. At system level, various fault-tolerant techniques have been proposed to correct the negative effects of SEUs. These techniques are applicable to processors and memory systems [6, 11, 7, 8, 12], and frequently they can be combined. For example, the use of error control codes (ECCs) has been found to be particularly useful for detecting/correcting SEU induced bit-flips in memory systems. However, ECCs guarantee the correction/detection of a limited number of errors, i.e. some faults may result in a number of errors in excess of the provided ECC ability. Thus, an improvement in reliability and/or availability over a long mission time (as figures of merit of a system) may require the concurrent use of multiple techniques; for example, ECCs could be combined with a high level of redundancy (such as a N-modular scheme) to overcome a large number of physical faults and system errors. The use of multiple techniques is often encountered through the utilization of dynamic arrangements by introducing features such as disagreement detection and fail-safe operation by using an appropriate decision circuitry.

A well known modeling technique for evaluating reliability and availability of multiprocessor [7, 8] and memory systems [11] with redundancy is based on Markov chains. A Markov chain model is a directed weighted graph in which each node represents a possible state of the analyzed system and each arc represents a transition [7, 8]. The weight of an arc is given by the rate of the process (such as failure or repair) by which the source state is left for a destination state.

In this paper, we analyze the reliability and availability of different fault-tolerant memory systems which are modeled by means of Markov chains in the presence of errors (caused by bit-flips due to SEUs). In particular, three different dynamic arrangements based on both hardware redundancy and the use of ECCs are proposed; novel state diagrams are introduced by which the decision circuitry (referred to as the arbiter) exhibits dynamic behavior in the arrangement of the redundancy (duplex versus triplex) and the correction/detection capabilities of the codes. Both reliability and availability are evaluated and compared. A reliability analysis of some of these systems has also been proposed in [12]; however differently from the proposed work, [12] is based on a static probability model. Also, different assumptions are made about the operation of the fault-tolerant arrangements. In this work we consider dynamic and strict requirements (i.e., if an error is discovered, the systems may reside in a "fail" state, thus requiring the use of an arbiter). This is different from [12], in which the voter of the redundant structure gives an output independently of the nature of the faults/errors, i.e. the discovery of mismatching words and error recovery capabilities are not explicitly dealt in [13].

This paper is organized as follows. Section 2 presents an overview of fault-tolerant systems with particular emphasis on dy-

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namic operation; Section 3 introduces novel Markovian models for the memory system. Section 4 presents the reliability and availability analysis and related issues. Results obtained for these three fault-tolerant modular schemes are compared. Conclusions of this work are then outlined in Section 5.

2. System Overview

This section presents the high level description of the fault-tolerant memory systems analyzed in this paper (Fig. 1), their Markov models will be described in more detail in Sections 3.1, 3.2 and 3.3 respectively.

Dynamic fault-tolerant schemes for memory systems differ from their traditional (static) counterparts due to the presence of extensive capabilities in their operation. These capabilities relate replication by modular redundancy (either duplex or triplex) to the generation of a correct system output. Error detection and correction as well as disagreement detection and voting are examples of capabilities which are utilized in a dynamic fault-tolerant system to adaptively operate over a long mission time. For example if a number of faults (due to SEUs) in the modules results in a large number of errors, a dynamic system may resort to a fail-safe status in the output (if indeed possible). These facilities are provided in hardware through a so-called arbiter where voting and coding circuits can be embedded.

In this paper three dynamic arrangements of a memory system are presented. First, a triplex system is considered (Fig. 1), made by the triplication of a memory module with no control code. The outputs of the three memory modules are collected by an arbiter. The arbiter compares the words received from the three memory modules and proceeds as follows:

- If the three words are equal (majority of 3), then it produces one of them as its output (no error/fault present).
- If a majority of two is present, then this is provided as output; a flag is set requiring repair for the disagreeing module (by one of the three pair-wise disagreement detectors).
- If there is total disagreement among the three words (i.e. none of them are the same), an undetermined output is provided; however, a flag is raised to indicate that a system failure has occurred. Note that in the triplex system, no fail-safe output is generated as it is assumed that the arbiter does not have this capability.

A duplex system (Fig. 1), based on the duplication of the memory modules making use of an EDC (*h-Error Detection (n,k) Code*) and an arbiter, is then considered. Different detection capabilities have been considered by varying the number of detectable bit-flips (i.e. h=1, 2, 3). The arbiter decodes the words from the two memories to detect possible errors. So, it operates as follows:

- If no error is detected for the two words (i.e. both correspond to the same codeword and a non-detectable error has not occurred by moving one of the two words to a different codeword) then the unique word is the arbiter and system output.
- If one of the two words is detected to have an error, then the other is produced at the output.
- If both words are found to have an error, then the arbiter does not produce an output and an error flag is set for fail-safe operation.
- If both words are found to have no error but they are not the same, then the arbiter does not produce an output and an error flag is set for fail-safe operation. This occurs if the number of flipped bits is greater or equal to the Hamming distance of the code. In this case, a non-detectable error has occurred, thus changing a word into a different codeword.

Eventually, a duplex system (Fig. 1) using a SEC-DED code (*Single Error Correcting-Double Error Detecting*) is introduced. This is based on the duplication of the memory modules by making use of a SEC-DED code with an arbiter as decision circuit. This circuit first reads and decodes the two words to detect errors, and when possible, it corrects them. Subsequently, the arbiter proceeds as in the previous case (using EDC).

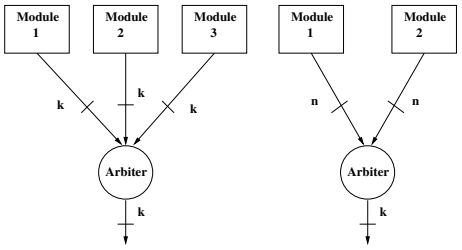

Figure 1. Block Diagram of the Fault-Tolerant Memory Systems

3. Markov Modeling

Initially the following definitions are introduced.

Definition: Reliability is the probability that the system produces a correct output at time *t.* [4]

Definition: Availability is the probability that the system is working at time *t.* [4]

Definition: λ is the fault exposure (or rate) of a single flipped bit (i.e., SEU on a single bit).

The systems considered in this paper have been modeled using Markov chains. To limit the often encountered problem of state explosion associated with Markov models of large and complex systems, an hierarchical approach has been used; the models deal with a very low level of the system hierarchy (the highest being the memory itself), i.e. a word of a memory module and its corresponding copy (copies) in the other module(s) of the duplex (triplex) system. However, its extension to higher levels (for example by considering all affected memories) is straightforward and the provided model does not affect its ultimate correctness.

The following possible system operations and events have been considered as causing transitions in the Markov state diagrams:

- A bit-flip (due to SEU) may occur in a word. This occurrence leads the system to move to a neighboring state in which the effect of the bit-flip is considered.
- A write operation in the memories leads the system to the initial operative state (fault-free by assumption).
- A read operation in the memories leads the system to either a safe transient state, or a fail state, depending on the number

of errors which have occurred at that time and the corrective capabilities of the system.

- A repair operation (such as replacement of a faulty memory module) is applicable as result of a flag being set. This operation moves the system from a state in which a correct read operation was made (despite the presence of an erroneous word in a module) to the initial state (no bit-flip).

Hereafter in the state diagrams of the Markov models, each transition will be labeled by its rate. Slow transitions are characterized by an exponential probability distribution function with rate λ, while fast transitions are characterized by a rate given by $\frac{1}{\mu}$ (for the particular memory location). In this model, fast and slow transitions will be easily distinguished, even though in the simulation (as described later) both of them are exponentially distributed.

The following additional assumptions are considered:

- Masking errors are not considered; these are those errors in which the words stored in the memory modules result in the same codeword (which is different from the correct one). This is unlikely to occur in practice; however, the Markov model is amenable to handle also this case with due modifications. In particular, also multiple flips on the same bit are not considered.
- As in previous works in the technical literature, the arbiter (as decision circuit) is always assumed to be error-free (i.e. it is a hard core component).

3.1. Triplex System

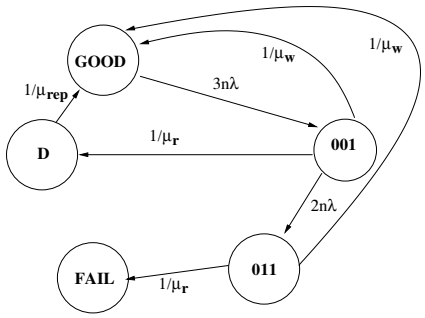

Figure 2. Markov chain model for Triplex System.

Fig. 2 shows the Markov chain model for the Triplex System; note that label "1"/"0" means that the considered word has (not) an error, respectively.

The states can be described in more detail as follows.

GOOD- The "GOOD" state is the initial state. By assumption, the system is error-free. A transition to the "001" state occurs with rate $3n\lambda$ as a consequence of a bit-flip due to SEU.

001- In this state, the triplex system has two error-free memory modules, while the third module presents an erroneous word. A second bit-flip due to SEU on a different module (at a rate given by $2n\lambda$) causes a transition to state "011". Otherwise, a read operation (occurring with rate $\frac{1}{\mu_r}$) moves the system to state "D".

D- The system enters the "D" state after a read operation, thus resulting in a correct system output, but one of the words stored in the memories has erroneous bits. In this state, the system is considered down (inoperative) till a *repair* (corrective) operation is performed. This operation is described by a fast transition, with rate $\frac{1}{\mu_{rep}}$ and can be considered as a recovery mechanism which takes place after a warning signal is generated by the arbiter.

011- This state is reached when the memory system has two modules with erroneous words. A read operation leads the system into the "FAIL" state.

FAIL- The "FAIL" state is reached when three different words are present at the arbiter's inputs, thus making impossible to generate a correct output.

Note that from both "011" and "001" a write operation (characterized by a rate $\frac{1}{\mu_w}$) takes the system to the "GOOD" state.

3.2. Duplex System with EDC

A duplex system making use of a disagreement detector (arbiter) and a circuitry implementing a h-Error Detecting (n,k) code, is considered next. Fig. 3 shows the Markov chain based model; a 2-bit EDC is applicable to this figure (note that "0", "1" and "2" mean a fault-free word, 1 bit-flip and 2 bit-flips, respectively).

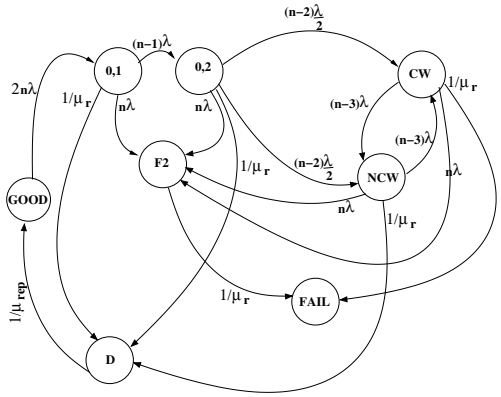

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Figure 3. Markov chain model for a duplex system with a 2-Error Detecting (n,k) Code

Some transitions have been omitted for readability: corresponding to a write operation, each state (except for "FAIL" and "D" state, as result of already performed read operations) has a fast transition to the initial state "GOOD" with rate $\frac{1}{\mu_w}$.

Each state can be described as follows:

GOOD- This is the initial state. By assumption, the system is error-free. The system can be moved to state "(0,1)" with rate $2n\lambda$.

(0,1), (0,2) These are intermediate states in which one of the two memory modules is fault-free and the other presents one or two flipped bits, respectively.

Different cases are possible for moving out of each of these states. From each of the two states, with rate $n\lambda$, the system reaches state "F2" as a consequence of the occurrence of a bit flip

in the previously fault-free word. In this case, the arbiter is now unable to produce a correct output. Instead, a read operation results in a correct output, leading the system to state "D". The duplex system is then in a wait (non-operational) state until repair is performed on the erroneous module.

Otherwise, the system can move with rate $(n-1)\lambda$ from state "(0,1)" to "(0,2)". This corresponds to a further bit-flip occurring in the already erroneous word.

Eventually, from state "(0,2)" the system can move both to the "CW" and "NCW" states with rate $(n-2)\frac{\lambda}{2}$. The former transition is due to a new bit-flip in the already erroneous word, thus changing it into a codeword (which is however different from the originally stored one). The latter case is due to the occurrence of a bit-flip leading to a non-codeword.

CW, NCW - When in these states, the system has one error-free word and an erroneous word. The latter word may belong to the codeword space depending on the number of erroneous bits and the code which is employed. These states are connected with transitions characterized by a rate given by $(n-3)\lambda$. This is an approximation introduced in the model, i.e. the likelihood of a transition should be proportional to $(n-e)$ (where e is the number of bit-flips which have already occurred in the erroneous word). The transitions between these two states reflect the case of reaching a codeword or a non-codeword after d-bit flips (where d is the Hamming Distance of the code). This approximation has been made to keep a reasonable number of states in the Markovian model.

From both the "CW" and "NCW" states, an error in the fault-free module takes the system (at a rate $n\lambda$) to state "F2". As for a read operation, it causes a transition to the "FAIL" state if performed while the system is in the "CW" state and to the "D" state if the system was in the "NCW" state. The "CW" to "FAIL" transition reflects the ability of the dynamic fault-tolerant system to give no output once two different codewords are read from the memories. In this case, the arbiter will also set an error flag (instead in [12], the voter is assumed to produce always a word at its output, so that there is 50% probability that it could be incorrect).

D- A read operation takes the system to the "D" state if (a) one memory contains the original codeword, and (b) the other memory contains a word which is not in the codeword space. In this state, the system is not operational till repair is performed. Then, the system moves to the initial "GOOD" state.

F2- This state is reached when the system can not operate correctly (i.e. independently of a sequence of transitions) following a read operation, i.e. either it does not produce a word at its output, or it generates an incorrect word. This is applicable when (a) none of the two copies of the same word in the modules is a codeword, or (b) one copy is a codeword and the other copy is not (in this case, the codeword is not correct), or (c) both modules generate different incorrect codewords.

FAIL The system can reach this state from the "F2" or "CW" state. As previously described, a system failure occurs when either the incorrect output is produced, or two different codewords are present at the arbiter's inputs.

3.3. Duplex System with SEC-DED

Fig. 4 shows the Markov model for a duplex system which employs a SEC-DED code.

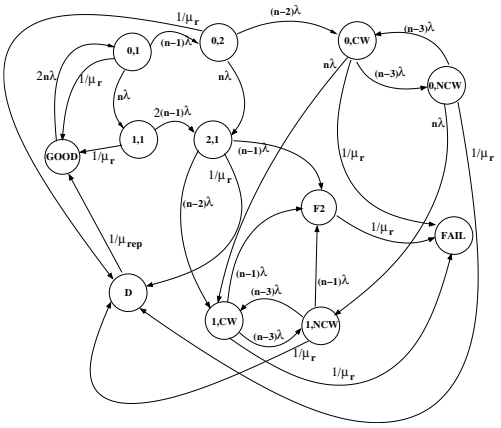

Figure 4. Markov chain model of a duplex system with a SEC-DED Code.

As in the previous model, Fig. 3 does not show (for readability purposes) the transitions to the initial "GOOD" state caused by a write operation (characterized by a rate given by $\frac{1}{\mu_w}$). As for notation, the labels "0", "1" and "2" still represent the number of bit-flips in the corresponding word of a given state.

In the transition diagram, the states "GOOD", "FAIL", "D" , "F2" are analogous as described in the previous subsection, and their description is thus omitted. The remaining states can be described as follows.

(0,1), (0,2)- These states have been also defined previously for the duplex system with EDC. However, the transitions are changed as follows: from the "(0,1)" state with rate $n\lambda$ the system goes to state "(1,1)" and with rate $(n-1)\lambda$ to state "(0,2)". Due to the 1-bit correction ability, a read operation from "(0,1)" makes the system return to the "GOOD" state. Otherwise, a read operation from "(0,2)" causes a transition to state "D". As the Hamming distance of a SEC-DED is four (i.e. h=2, d=4), a further bit-flip in the already erroneous word (occurring with rate $(n-2)\lambda$) takes the system to state "(0,CW)", in which one of the memory modules is error-free and the other generated an erroneous codeword due to an erroneous correction (i.e. a correction to a codeword different from the original one). Eventually, at a rate of $n\lambda$, the system moves to state "(2,1)".

(1,1)- In this state the words of both memory modules have only one erroneous bit (therefore they can be corrected). From this state, the system goes to the "(2,1)" state at a rate $2(n-1)\lambda$; a read operation causes a transition to the "GOOD" state.

(2,1)- In this state, one word has two flipped bits, while the other has only one. If a new bit-flip occurs in the module which has already two errors (with a rate of $(n-2)\lambda$) then the system goes to state "(1,CW)". In this case, the codeword in one of the two modules is erroneous due to an erroneous correction. Eventually, a read operation causes a transition to the "D" state because the word with only one erroneous bit can be corrected.

(0,CW), (0,NCW)- "(0,CW)" and "(0,NCW)" are analogous to "CW" and "NCW" of the EDC encoded duplex system. The difference is that a bit-flip in the error-free module (at a rate of $n\lambda$) causes a transition to states (1,NCW) and (1,CW) instead of the

"F" state. This reflects the 1-bit correction ability of the system. Again, the probability of bouncing between the two states is given by a SEU rate of $(n-3)\lambda$, approximated to the upper bound value.

(1,CW), (1,NCW)- The system enters these states when one erroneous bit on a word and multiple errors on the other occur, thus this latter word may or not belong to the codeword space. As for the "(0,CW)" and "(0,NCW)" states, they are connected through a transition at an approximate rate given by $(n-3)\lambda$. If another error occurs (at a rate of $(n-1)\lambda$) in the module with already one bit flipped, then the system moves to the "F2" state. Finally, a read operation from "(1,CW)" moves the system to "FAIL", because it is not possible to distinguish which of the two codewords is correct. Otherwise, a read operation from "(1,NCW)" causes a transition to the "D" state.

4. Analysis

The solution and evaluation of the proposed Markov models are accomplished by using the PAWS solver [9, 10]. The following considerations are applicable to the state transitions:

i) Transitions due to SEUs (i.e. slow transitions) are characterized by an exponential distribution [9, 11, 7].

ii) All other transitions are considered as fast transitions, thus characterized by a conditional mean transition time and standard deviation (as for the White's or Lee's methods of SURE [9]). This reflects the difference between the SEU rate and the rates by which all other operations may occur in the memories. However, PAWS [10] operates under the assumption that all transitions are modeled by an exponential distribution. Thus, the input values for the standard deviation are ignored and the exponential rate is given by $\lambda = \frac{1}{\mu}$, where μ is the conditional mean transition time. This approximation is introduced to maintain a realistic simulation time in the evaluation of the Markov models.

In the remainder of this section, results for reliability and availability are presented. In both cases, unreliability and unavailability (as the down-time probability) are reported for ease of presentation and readability.

4.1. Reliability

For the fault-tolerant systems analyzed in this paper, reliability has been computed as $1 - P(FAIL)$, where $P(FAIL)$ is the probability of being in the "FAIL" state (i.e. the state in which the system through its arbiter can not generate a correct output).

For the duplex system with EDC, three different cases have been considered, i.e. h=1,2,3 respectively. Note that previously in Section 3.2, only the case for h=2 has been shown in detail; however, the models for systems with 1-bit and 3-bits detection capabilities are similar.

The results given in Figs. 5, 6 and 7 show the unreliability of the fault-tolerant memory systems with respect to time, the simplex (non fault-tolerant) reliability, and the SEU rates, respectively. Fig.5 shows the simulation results for a fixed SEU rate of 10^{-4} SEU/hours, and for a time sweep from 0 to 20000 hours. As for the transitions, the following values have been used for the rates: i) for a write operation $\mu_w = 5 \times 10^{-4}$, ii) for a read operation $\mu_r = 10^{-4}$, and iii) for repair $\mu_{rep} = 8 \times 10^{-4}$.

The evaluation of the Markov models shows that the unreliability of the triplex system is higher than for both duplex arrangements. This occurs due to the limited capabilities of the arbiter in the triplex system (for example no fail safe operation in the output). As for EDC based systems, no significant difference for the cases $h = 2$ and $h = 3$ has been observed in the simulation, resulting in very close plots in Fig.5. The unreliability of the SEC-DED system results in the lowest values among the proposed models, i.e. this system has the highest reliability.

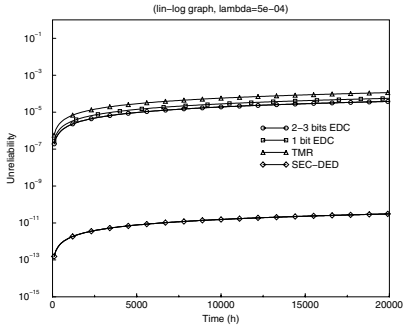

Figure 5. Unreliability versus time

Fig. 6 shows in a lin-log plot the unreliability of the three fault-tolerant memory systems versus that one of a simplex system for a fixed λ. The same parameters as before have been used.

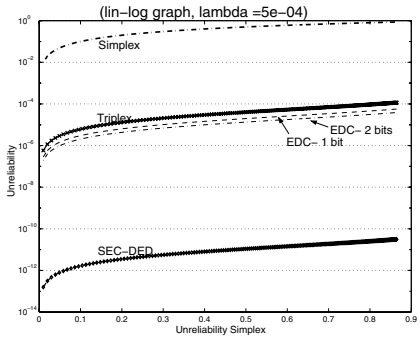

Figure 6. System unreliability versus simplex unreliability

Furthermore, Fig.7 shows in a log-log plot the unreliability of the three fault-tolerant memory systems by varying λ (in the range between 10^{-10} and 5×10^{-1}). The observation time has been fixed to one year; for the fast transitions the same values as previously given have been used. Fig.7 shows that the reliability of the duplex system with SEC-DED is higher than those of the other two fault-tolerant systems analyzed in this paper. Fig.7 also shows that the unreliability saturates faster for the triplex memory system than for two duplex arrangements with coding.

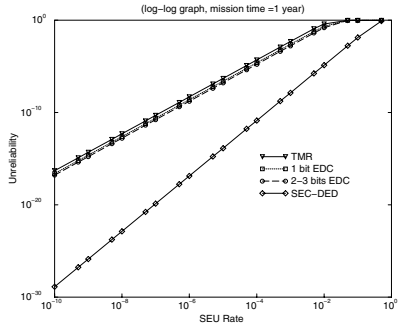

Figure 7. Unreliability versus SEU rate

4.2. Availability

Availability has been evaluated as function of the mean time to repair (MTTR); similarly to the reliability case, the down-time probability (i.e. the unavailability) has been computed and plotted. The down-time probability is given by the sum of the probabilities for the system to be in the "FAIL"and "D" states, as described in sections 3.1, 3.2 and 3.3. When in these states, the system is considered by assumption to be down and a repair operation is required as corrective action (i.e. upon repair, the system reaches the initial fault-free state). Thus,the availability is given by $1 - (P(\text{“}FAIL'') + P(\text{“}D''))$.

The parameters used for these simulations are hereafter given: i) λ is fixed to 10^{-4}, ii) the observation time is given by $T = 1$ year, iii) for a write operation $\mu_w = 5 \times 10^{-4}$, and iv) for a read operation $\mu_r = 10^{-4}$. MTTR varies between 10^{-8} and 5×10^{-1}.

Fig. 8 shows the simulation results using PAWS. The availability of the duplex system with SEC-DED is higher (its down-time probability is lower) than those of the other two memory systems considered on this paper. As for reliability, the difference in availability between duplex systems making use of 2-bit and 3-bit codes for detection is not remarkable, i.e. by increasing the detection capability from two to tree bits for the duplex system does not significantly affect the overall system availability.

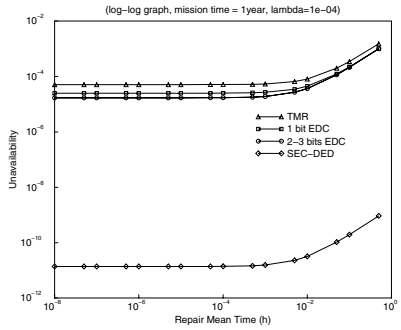

Figure 8. Down time (unavailability) vs time

5. Conclusions

This paper addresses the reliability and availability of three fault-tolerant memory systems in the presence of SEU. These fault-tolerant systems utilize modular redundancy (either duplex or triplex) and so-called dynamic capabilities (such as disagreement detection, fail-safe and coding) in their operation. In particular, a triplex modular system and two duplex modular systems making use of EDC and SEC-DED respectively have been considered. The systems have been modeled using a novel Markov chains which enable the dynamic modeling differently from previous work [12].

Reliability and availability of these models have been evaluated using the Markov solver PAWS. The results show that among the considered models, the use of a SEC-DED code with a duplex arrangements in the memory modules improves both availability and reliability compared with a system with higher modularity such as triplex.

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