Design of a QCA Memory with Parallel Read/Serial Write

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Abstract

This paper presents a novel memory architecture for implementation by Quantum-dot Cellular Automata (QCA). The proposed architecture combines the advantages of reduced area of a serial memory with the reduced latency in the read operation of a parallel memory. An extensive evaluation with respect to latency and area is pursued. For area analysis, a novel characterization which considers cells in the logic circuitry, interconnect as well as the unused portion of the Cartesian place as QCA layout, is proposed.

1 Summary and conclusions

Our proposed novel memory architecture for QCA implementation utilizes a parallel read operation on multiple bit loops. The memory arrangement is referred to as "hybrid" due to the different operational mechanism for the two memory operations (read and write). The proposed memory results in two advantages over previous architectures: (1) the parallel read mechanism allows a reduced latency compared with $O(N)$ latency for serial memories (where N is the number of bits in a loop.); (2) a reduced area is needed compared with a parallel memory, thus increasing the density of the memory (this is accomplished due to sharing of interconnects, the reduced control logic and a different loop implementation). The hybrid memory is best suited in application in which the memory is often read and seldom written. A novel figure of merit referred to as *effective area* is introduced in the analysis. The effective area is the geometric area of the memory layout which includes the area of the cells for the logic and interconnect circuits as well as the unused portion of the Cartesian plane (to avoid unwanted Coulombic interactions among cells). Different layouts of the hybrid memory are evaluated using this new metric.

2 Proposed memory architecture

The proposed memory architecture can be considered as an evolution of the serial memory presented in [1].

A block diagram of the proposed memory architecture is shown in Figure 2. In this Figure, m loops of $2^n = N$ bits are arranged to form a m bit word of $2^n = N$ locations which can be accessed in parallel. Each loop has as inputs the n bit address of the accessed bit and the following additional signals: (1) the ***R/W#*** control signal which specifies if the loop is accessed in a write or read operation; (2) the serial data input D_{in}; (3) a ***VALID*** control signal. The last signal is provided to each loop by the adder and allows the synchronization of the write operation. The write operation must be performed serially on the loops and thus, the correct bit must be addressed. For both the read and write operations, addressing the same bit independently of the configuration of the shift register requires the input address to be added to an offset (which is stored in a 2^n counter).

The operation of the hybrid memory can be described as follows: when a write is requested, this operation is performed provided the value of the "biased" address ***ADDR'*** is zero. When the NOR operation of the bits of the address is equal to one, then the write operation can have at most $(2^n - 1)$ clock cycles delay. If a read must be performed, the value of ***ADD'*** is directly provided to the 2^n-to-1 demultiplexers of every loop, thus incurring into an immediate (virtually zero delay) read operation for the addressed m bits word. The logic structure inside each loop is shown in Figure 1. The inputs of the loops are the m bits ***ADDR'***, D_{in}, ***VALID*** and the ***R/W#*** signals, while the output is the D_{out} signal. The write logic circuitry provides the inputs to the majority voter (MV) to either change the value of the stored information (placing the same new data at two of the three inputs), or leave it unchanged (placing a 0 and 1 at two inputs). The output (read) logic circuitry places the value of the addressed bit on D_{out} if the read operation is selected, 0 otherwise.

3 Comparison

In this section, the proposed architecture is evaluated in terms of latency and area and compared with previously proposed QCA memories. The metrics considered for com-

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parison are the read/write latency (compared to a serial memory) and area (compared to a parallel implementation).

Table 1 shows the qualitative features of the proposed memory architecture as well as the serial [1], parallel [3] and H Tree [2] architectures.

	Advantages	Disadvantages
Serial	Density	Read/write Latency
Parallel	Read/Write Latency	Area Density (small size)
H Tree	Density	Read/Write Latency Unconventional access
Hybrid	Read Latency and Density	Write Latency

Table 1. Comparison

For the read operation, the proposed memory improves over a serial memory as it has a virtually zero latency, while for the write operation, the proposed architecture has the same performance as a serial memory with a loop of equal size. The difference between latency of the two operations (read and write) suggests that the proposed hybrid scheme is better suited to applications in which memories are seldom written and often read. The area of the proposed hybrid memory is reduced compared with a parallel architecture due to the presence of decoding logic circuitry in each memory loop; however, some modifications in the layout can be implemented to allow sharing of duplicated resources between different loops. The proposed hybrid memory allows to store more than one bit per loop, thus reducing the number of required loops compared to a parallel memory. Therefore, the area of the proposed memory improves over a parallel arrangement for small memory size. For larger sizes, the repetition of decoding logic circuits reduces the improvement.

3.1 Latency

The proposed hybrid approach combines the area efficiency of a serial memory [1] with a reduction in latency for the read operation (which is performed in parallel). An estimate of the latency is performed by evaluating the complexity of the algorithm which describes the steps involved in the read and write operations. The read and write operations of a serial memory are comparable to a serial search of a list of N elements, where $N = 2^n$ are all the addressable locations in the memory loops. This has a complexity (and therefore a latency) of $O(N)$ as requiring $N/2$ number of accesses on average. The read and write operations for the proposed memory are different. By avoiding the loop for an average of $N/2$ clock cycles for the read operation, this allows a constant latency (immediate access) which is not related to the dimension of the loop.

3.2 Area overhead

The area required by a QCA based architecture is related to the number of QCA cells needed for its implementation. However, differently from a transistor based design, the number of cells are not only those realizing the desired logic functions but also those used for the interconnect. Moreover, such analysis must also take into account the area that is left unused in the layout. The unused portion of the area is needed to limit the Coulombic interaction between QCA cells in different parts of the circuits. Therefore, a computation of the area must take into account the geometric area occupied by the QCA circuit, i.e. the sum of the area occupied by the cells (implementing logic functions and interconnect) and the unused portion. This total area is referred to as the effective area. In the analysis, the effective area is calculated for evaluating and comparing the proposed memory architecture. Let d be the lateral dimension of a QCA cell and n_x and n_y be the count of cells in the x and y dimensions of the plane, then the effective area of a QCA layout is given by $A = (n_x d) \cdot (n_y d) = A_u + A_{un}$ where A_u (A_{un}) is the used (unused) portion of the layout area occupied by the QCA cells in the logic and interconnect circuits. The following layouts have been compared and the results are summarized in Tables 2 and 3: 1×4 parallel architecture (Figure 3); 1×4 hybrid memory (Figure 4); 4×4 parallel memory; 4×4 hybrid memory generated by modular replication of the layout in Figure 2; H Tree based 4×4 hybrid memory (Figure 5).

It can be noticed that the layout of the hybrid memory 1×4 is only 32% of the layout of the parallel memory architecture due to the following reasons: (1) the loop structure is realized in a small area; (2) the control logic is shared between the four bits. Moreover, noting that the effective area of the 4×4 memory is more than four times larger than the area of a 1×4 memory a H Tree based arrangement as in Figure 5 can be used in the design of the hybrid memory to share the signal routing resources. Let R=A_m/A_{par} where A_m (A_{par}) is the effective area of a specific memory architecture (parallel memory). Table 2 summarizes the effective areas and the ratios for the memories analyzed and compared in this paper. An increase in memory size reduces the saving accomplished by using the proposed architecture due to the decoding logic for each loop. As a final remark Table 3 consider the ratios of A_u and A_{un} for the previously introduced layouts. A_u varies from 24% to 32.5% *i.e.* A_{un} accounts for the larger portion of effective area.

References

[1] T. Berzon, D.and Fountain. A memory design in qcas using the squares formalism. In *Proceedings. Ninth Great Lakes Symposium on, '00*, pages 166 – 169, Mar 1999.

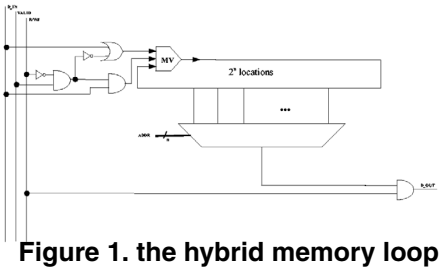

Figure 1. the hybrid memory loop

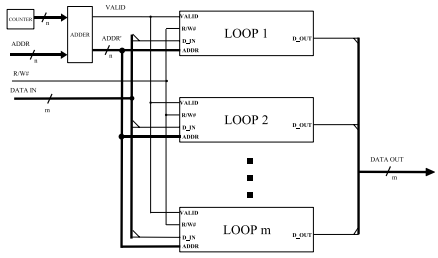

Figure 2. scheme of the hybrid memory

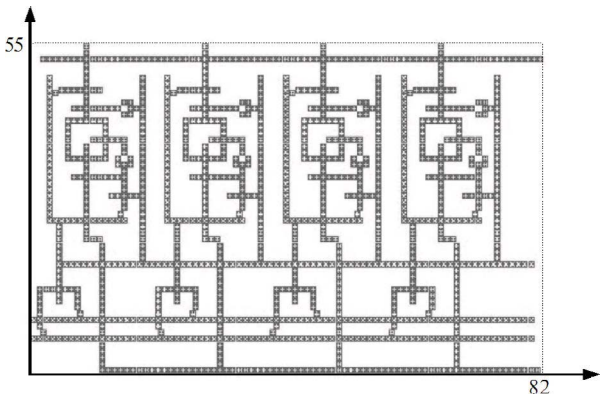

Figure 3. Layout of a 1×4 parallel memory

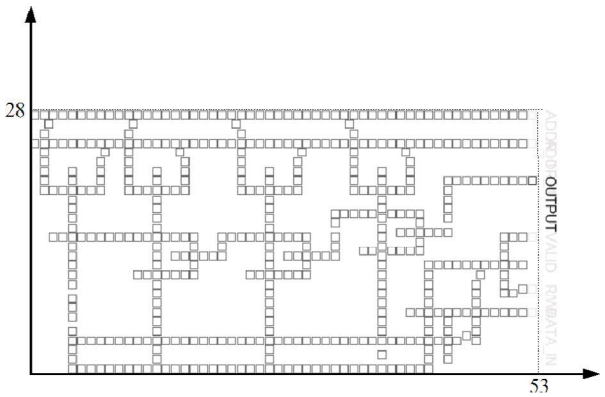

Figure 4. Layout of 1×4 hybrid memory

	$A_{hyb}\mu m^2$	$A_{par}\mu m^2$ *same size*	R
1×4	0.148	0.455	32%
4×4	1.36	1.63	80%
4×4 *H Tree*	0.676	1.63	41%

Table 2. Area Comparison

	A	A_u	A_{un}	$A_u\%$	$A_{un}\%$
1X4 PAR	0.451	0.124	0.326	27	73
1X4 HYB	0.148	0.0481	0.1	32.5	67.5
4X4 PAR	1.63	0.392	1.24	24	76
4X4 HYB	0.792	0.233	0.558	29.5	70.5
4X4 H Tree	0.676	0.183	0.49	27.1	72.9

Table 3. Comparison of A_u and A_{un}

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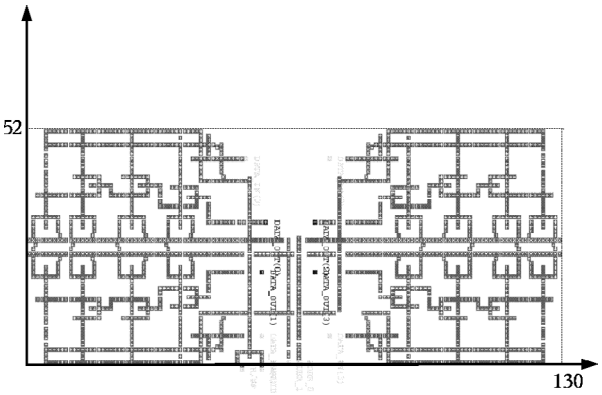

Figure 5. H Tree structure layout of a 4×4 hybrid memory