Localization of faults in Radix-n Signed Digit Adders

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***Abstract*— It is widely known that a adder can be checked by using check symbols that are residues of the numbers modulo some base. This paper extends this characteristic to a radix r Signed Digit (SD) representation. The confinement of the carry operation can also be exploited to localize the faulty resources in the SD adder and to reconfigure the adder in order to work with a reduced dynamic range. The fault localization procedure is presented in this paper and the reconfiguration the SD adder after the fault localization is discussed.**

I. Introduction

In the literature a number of self-checking adder implementations have been proposed, but not many works propose adders which provide combined error detection and correction capabilities. The most widely applied techniques to obtain error correction in adder circuits are based on time-redundancy [1], or on the residue number system representation [2], [3]. In [4], [5] we propose a parity check scheme for radix-2 SD adders that allows the fault localization and the graceful degradation of the faulty adder. Instead, our solution proposed in [6] is based on generic r-radix signed digit representation and the correctness of the adder operation is checked using a residue of the input operands. The goal of this paper is to extend the work presented in [6] discussing the localization of a faulty resource in a SD adder and to propose a graceful degradation approach to reconfigure the SD adder using the remaining fault free resources. We remark that differently from [4],[5] the method proposed in this paper is suitable for a generic r radix SD representation and both the fault localization and the graceful degradation approach can be achieved with less complexity than the algorithm proposed in [4],[5]. The paper is organized as follows: in section II a background of r-radix SD arithmetic is given and the error detection method is presented for the adder operation. Section III provides a discussion of the different cases of fault localization and shows the related algorithm. The proposed graceful degradation approach is presented and a comparison of this method with the procedure proposed in [4],[5] is provided. Finally, in Section IV, the conclusions are drawn.

II. Background

In a radix r SD representation a number x can be represented as

$$x = \sum_{i=0}^{n-1} x_i r^i \tag{1}$$

Where the digit set is $x_i \in \{-a, \ldots, -1, 0, 1, \ldots, a\}$, with $\left\lceil \frac{r-1}{2} \right\rceil \leq a \leq r-1$.

In fact, given two operands a and b the addition operation can be split in the two operations

$$w_i = a_i + b_i - rc_i \tag{2}$$

$$z_i = w_i + c_{i-1} \tag{3}$$

where

$$c_i = \begin{cases} 1 \, if \, (a_i + b_i) \geq a \\ -1 \, if \, (a_i + b_i) \leq -a \\ 0 \, if \, |a_i + b_i| < a \end{cases} \tag{4}$$

being $w_i \in \{-a+1, \ldots, -1, 0, 1, \ldots, a-1\}$ an auxiliary variable. This representation allows to implement a carry-free adder using a block ADD1 for the equations (2) and (4) and a block ADD2 for the equation (3), connected like described in fig.1a. The correctness of the SD adder operation can be evaluated using check symbols that are residues of the numbers involved in the operation modulo some base. The check symbols are able to detect any kind of fault inside the adder if the erroneous value have the check symbols different from the ones of the faulty free operation. For an adder with the check symbol based on residue codes this consideration can be written as:

$$< a + b >_m \neq < a + b + e >_m \Rightarrow < e >_m \neq 0$$

Where $< \cdot >_m$ is the modulo m operation, a and b are the operand of the adder and $e \neq 0$ is the error due to a fault inside the adder. For a radix r signed digit adder the faults can occur in the ADD1 and ADD2 blocks of fig.1a. A fault in the ADD1 block (or in an input digit a_i or b_i) can change the values of the intermediate results w_i and c_i. If we define $\overline{w_i} \in \{-a+1, \ldots, -1, 0, 1, \ldots, a-1\}$ and $\overline{c_i} \in \{-1, 0, 1\}$ the faulty intermediate results, the error value can be computed as:

$$e = e_i r^i = e_w r^i + e_c r^{i+1} = (\overline{w_i} - w_i) r^i + (\overline{c_i} - c_i) r^{i+1} \tag{5}$$

with $|e_w| = |\overline{w_i} - w_i| \leq 2(a-1)$ and $|e_c| = |\overline{c_i} - c_i| \leq 2$. Therefore for e_i we obtain: $|e_i| \leq 2r + 2a - 2$.

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A fault in the ADD2 block can change the values of the result z_i to $\overline{z_i}$, the error value is $e = e_i r^i$ with $|e_i| \leq 2a$.

Now we can choose an integer m for which $< e >_m = 0$ iff $e = 0$. This condition allows to avoid the aliasing between the modulo m of a erroneous results and the correct one. The aliasing is avoided for all m for which

$$m > 2r + 2a - 2 \geq 2r + 2(r-1) - 2 = 4r - 4 \qquad (6)$$

Using $m = r^2 - 1$ equation (6) become $r^2 - 4r + 3 > 0$ that is satisfied for all radix $r > 3$. The implementation of the adder modulo $r^2 - 1$ can be done the end-around carry structure shown in fig.1b).

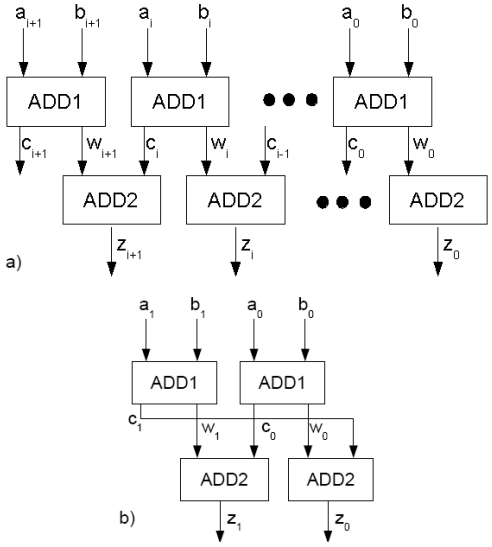

Fig. 1. a) Signed Digit Adder b) Signed Digit Adder modulo $r^2 - 1$

III. Fault localization procedure

In this section are introduced fault localization procedures for the r-radix adder when stuck at faults occur in different parts of it. To improve the clarity of exposition without loss of generality, we take as example an 8 digit adder. In the following we will show how the analysis of the erroneous behavior allows to identify the faulty digit. Depending on its location, different faults cause different effects which have been considered in the fault localization procedure as will be shown later. When an error is detected on the output the proposed fault localization procedure is started. Before introducing the fault localization procedure, we provide some useful definitions:

- define Right Shifted Inputs (RSI) of the new inputs given from the right shift of the inputs vectors by two positions and with the two MSB set as 0 $i.e.$ A^{RS}=$\{0, 0, a_6, a_5, a_4, a_3, a_2\}$ and Left Shifted Inputs (LSI) the new inputs given from the left shift of the inputs vectors by two positions and setting the two LSB as 0 $i.e.$ A^{LS}=$\{a_5, a_4, a_3, a_2, a_1, a_0, 0, 0\}$
- define Z^{RS}, Z^{LS} the results obtained using the shifted operands

The equality relation between Z and Z^{LS} is valid for $0 \leq i \leq 6$ while the same relation is valid for $2 \leq i \leq 8$ between Z and Z^{RS}. For the left shifted output the equality is not valid for z_7 and z_8 because two most significant digits are lost with the shift operation. For the right shifted output the equality is not valid for z_0 and z_1 and z_2 because two least significant digits are lost, and also their possible carry can be lost. It can be observed that the shifted inputs can activate again the error detection or not depending on the occurred fault. The effects of different types of faults are reported depending on the affected digits and/or the error detection signal. As stated above, the reported procedures are possible because of the carry free features of the signed digit arithmetic adders. The faults are divided into three types depending on the block affected by it. Type ADD1 and ADD2 faults affect the ADD1 and ADD2 blocks respectlively, and the error produced by this faults affects 2 or 1 digits respectlively. Instead, type 3 fault is related to a fault in the residue checker. Once an error is detected the operation is repeated with the left shifted inputs and the results Z_{LS} and Z are compared. If the new computation does not activate the fault we observe for $0 \leq i \leq 6$ the following behaviour: $z^{LS}_{i+2} = z_i$ for any digit that is not affected by the fault and considering j as the faulty slice in the SD adder we have $z^{LS}_{j+2} \neq z_j$ if the fault affects the ADD2 block and an additional inequality $z^{LS}_{j+3} \neq z_{j+1}$ if the fault affects the ADD1 block. From those inequalities we can localize the type of the faulty block (ADD1 or ADD2) and its location inside of the adder. This procedure provides also the correct digits z_j and z_{j+1} of the original operation (the non shifted one) as z^{LS}_{j+2} and z^{LS}_{j+3}, respectively. Instead, if the operation with the shifted operands activates the fault again we can observe up to four consecutive inequalities. Two of this inequalities are caused by the errors in the original operation and the other two are caused by the errors in the shifted operands. Anyway, the localization of the fault and correct digits of the original operation can be obtain with a procedure similar to the one reported above. In fact, if we suppose that the fault affect the j slice the inequalities $z^{LS}_{j+2} \neq z_j$ and $z^{LS}_{j+3} \neq z_{j+1}$ are caused by the errors in the digits z_j and z_{j+1} while the inequalities $z^{LS}_{j+1} \neq z_{j-1}$ and $z^{LS}_{j} \neq z_{j-2}$ are caused by the errors in the z^{LS}_{j} and z^{LS}_{j+1} digits. Therefore, also in this case the correct digits z_j and z_{j+1} of the original operation (the non shifted one) are z^{LS}_{j+2} and z^{LS}_{j+3}. This procedure in valid for all the faults affecting the slices with $0 \leq i \leq 6$. For the remaining slices the procedure with the LSI operands do not provide any inequality and a similar procedure that uses RSI must be performed. Finally, we remark that the fault in the checking blocks of the SD adder can be identified if no inequalities are reported after the computation with either the LSI and RSI operands. In this case the result of the operation is always correct, but the checking capabilities of the system are lost. The algorithm of fault detection, localization and correction is summarized in the graph reported in Fig. 2.

Note that in Fig. 2 the exit conditions on the leaf nodes are alwais on a fault detection event. The graceful degradation

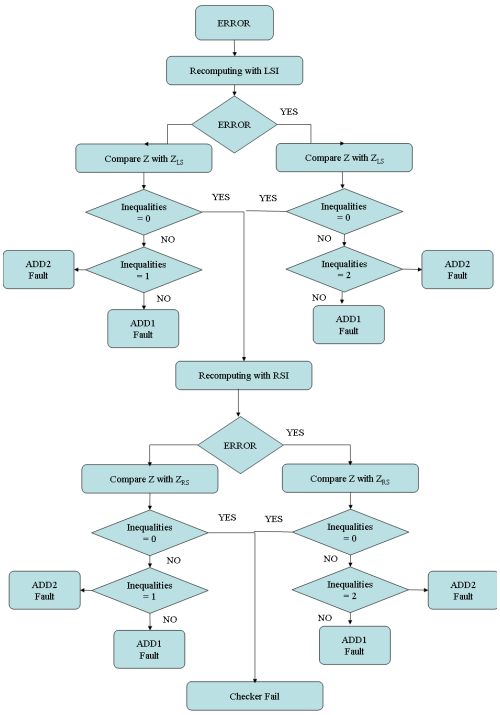

Fig. 2. Fault localization algorithm

capabilities of the adder are related to two main aspects of this algorithm: first of all the algorithm always allows to detect and localize the fault, and to obtain the correct output comparing the result of the operation with LSI and (if needed) with RSI operands. Moreover, as a further graceful degradation feature, the fault localization allows to use the adder with a reduced dynamic. In fact, assuming that $x \in \{1, 2\}$ faulty digits are detected a 8 digits adder, it can still be used as a $(8-x)$ digits adder applying suitable modifications to the input vectors A and B. For instance, if the digits $\{3, 4\}$ of the adder are faulty, the six digit input vectors starting from the 8 digits inputs should be set up as follows

- $A = \{a_5, a_4, a_3, a_2, 0, a_2, a_1, a_0\}$
- $B = \{b_5, b_4, b_3, b_2, 0, b_2, b_1, b_0\}$

While the output with reduced dynamic is:

$$Z = \{z_6, z_5, z_4, z_3, -, -, z_2, z_1, z_0\}$$

The above reported example is related to a type ADD1 fault in the $i = 3$ digit. Because of the assumptions obtained by the fault localization procedure the digits $\{0, 2\}$ and $\{5, 8\}$ are not affected by the fault. Therefore, in order to compute correctly the z_3 output the digits a_2 and b_2 are repeated in position 5 to provide the correct carry to the ADD1 block in position 6.

The differences between the method exposed and the algorithm originally proposed in [4] are related to the confinement of the carry propagation. In fact, to realize carry confinement in radix-2 SD adders the method proposed in [7] must be used. This method implies that the errors produced by a fault can propagate to up to 3 output digits differently by the r-radix SD adder in which the maximum propagation is of only two digits. This difference implies that:

1) the identification of the fault in the radix-2 SD adder requires the introduction of four types of fault and consequently a more complex fault localization algorithm.
2) To avoid aliasing in the results of original and shifted operands a shift of 3 digits must be performed. Therefore the procedure for radix-2 SD adders can be applied only if a wide number of digits is used.
3) In r-radix SD adders the reconfiguration after fault localization exludes only two digits, while in [4] the exclusion of 3 digits must be taken into account.

IV. Conclusions

This paper has presented a methodology to check the correctness of radix r signed digit adder operation. Exploiting the carry free property of the SD adders an error due to a stuck-at in the adder can be easily detected using two check symbols. SD adders show properties that allows to extend the methodologies based on residue codes to a r-radix signed digit representation. Differently from previous presented works, the adoption of an r-radix SD representation permits a reduction of the complexity of the localization algorithm and a more efficient confinement of the effects of a fault. A self-checking implementation of the SD adder is illustrated and the algorithms to achieve error correction, fault localization and graceful degradation are proposed. The main idea is to take advantage of the confined carry propagation in SD adders. This characteristic has been used to perform an error propagation analysis and to set up localization and correction procedures. The proposed algorithm localizes the faulty digit(s) by means of a recomputation with the shifted operands method. After the fault localization a reduced dynamic approach allows to obtain the result of the adder operation with fewer output digits.

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