# On the Effects of Intra-Gate Resistive Open Defects in Gates at Nanoscaled CMOS

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***Abstract*—This paper presents a detailed characterization of the effects of intra-gate resistive open defects on nanoscaled CMOS gates as causing faults with timing and pattern sequence dependency. The values of the least detectable resistance are established for different feature sizes using HSPICE. It is found that as the feature size is reduced, the value of the least detectable resistance increases in the presence of a fault resulting in a delay of less than one nanosecond. The use of a low voltage testing technique is investigated for the detection of these faults. Finally, an analytical model that takes into account the gate current is proposed; this model considers the pronounced effect of the gate current at a decreasing feature size, while incurring in a small error compared with simulation results.**

## I. INTRODUCTION

With the decreasing scaling of feature size in VLSI technology, the effects of manufacturing defects cannot be only modeled by conventional stuck-at and transition faults; more attention is being devoted to so-called Small Delay Faults (SDF) as caused by the sum of delays induced by resistive defects. This paper focuses specifically on the detection of resistive open defects. A resistive open defect [1] is a defect arising when two points are connected by a finite amount of resistance. Examples of resistive open defects are thin wires, ill-formed contacts (vias), or cracks in silicides [2] [6]. Unlike a full open defect, this fault cannot be detected using standard stuck-at test vectors; moreover, it is also difficult to detect resistive open defects using IDDQ as well other techniques [2][8]. Test vectors generated under a transition delay fault model in which slow-to-rise and slow to-fall faults are assumed on the output signal of logic gates, do not guarantee the detection of all intra-gate level faults because they consider only the input and output terminals and not the fault sites inside a gate. The resistive open defect does not change the output state, but it only introduces a small amount of delay [7]; a so-called *small delay fault* is a fault that causes a delay of less than one nanosecond. In this paper, the small delay will be determined for the resistive defect inside the gate (i.e. intra-gate).

[1] has studied the effects of intra-gate resistive open defects on small delay faults in different basic gates at 180nm feature size; the effect of different input vectors has been observed on the output delay for faults at different sites. The fault coverage is then obtained for the basic gates. [1] has proposed three different fault models, i.e. intra-gate resistive open, intra-gate open and input-port-oriented transition faults. In [2], a simulator has been proposed for the resistive open defect by taking into consideration the probabilistic coverage of the resistance. In these approaches, the resistance is considered only on the nets and intra-gate resistive faults are not considered; moreover, they consider the delay and timing constrains at gate level. So, emphasis is mostly placed on the timing delay than the detection of the resistance values because the model establishes the delay based on the characteristics of the fault free circuit, the capacitance and the resistance. Since the intra-gate resistance is not considered, the fault coverage attained by this approach is not high.

In this paper, we study the effects of an *intra-gate* resistive open defect with technology scaling below 180 nm by simulation based on predictive technology models (PTM) and investigate the use of a low voltage testing technique to increase the fault coverage. Finally we propose an analytical model to evaluate the minimum detectable resistance of the intra-gate resistive open defect. The paper is organized as follows: Section II provides an overview of the simulation setup, Section III reports the results of the simulation on different feature sizes and circuits; Section IV analyzes low voltage testing. An analytical model is presented in Section V and the results of this model are compared with the simulated ones. Finally Section VI concludes the manuscript.

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## II. Simulation Setup

In this paper, simulation has been conducted using the Predictive Technology Model (PTM) at different technology nodes [10]; simulation is based on the BSIM4 standard MOSFET model. A fan out of 4 is connected as inverter(s) at the gate output. The supply voltages for 180nm, 90nm, 65nm, 45nm and 32nm are given by 1.5V, 1V, 0.8V, 0.7V and 0.6V respectively. Moreover a Wp/Wn of 2:1 is used in the gate design at a nominal temperature of 25C. The gates have been initially simulated and proved to be working correctly; then the netlists for the gates (obtained from Cadence) have been simulated in HSPICE at different sizes for nanometer technologies. The input is a pulse with a rise time (from 0 to Vdd) of 1ns (this is also applicable to the fall time). Initially, an inverter (INV) gate has been designed at 180 feature size. The fault free circuit has been simulated using HSPICE; the delay was found to be less than one nano second. Then, faults have been introduced in the inverter (at different sites as shown in Fig.1 a). Using a similar process, faults have been injected at different nodes in the NAND and NOR gates (as shown in Fig. 1.b) and Fig. 1.c)).

For fault simulation, the value of the resistance at a specific site has been increased in 50 kΩ steps till the delay at the output terminal exceeded the 1ns limit. The value of the resistance for which the delay exceeds 1ns, is considered to be *the least detectable value* (also referred to as *minimum*) for the given site (under the provided vector(s)). At 180 nm feature size the largest resistance value that was applied, is 50 MΩ. If the resistance value exceeds 50M and the delay is still not larger than 1ns, then that fault is considered to be undetectable.

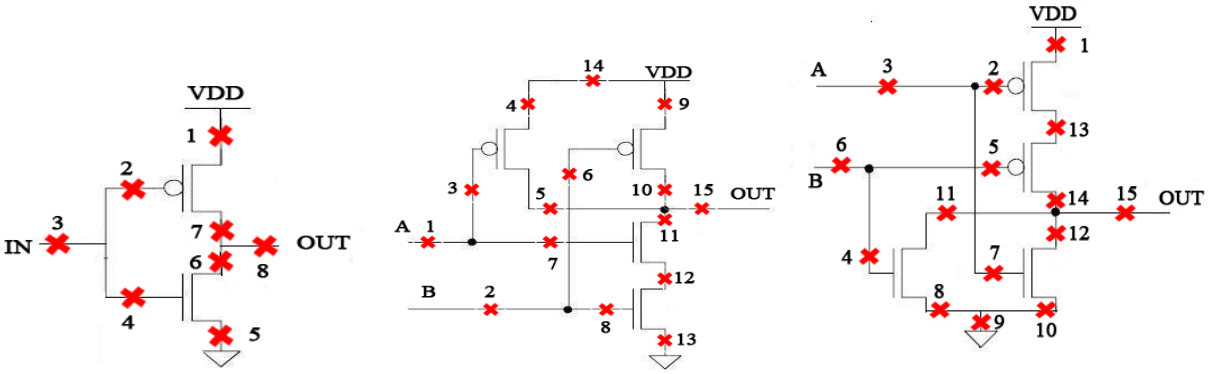


**Fig 1: a) Resistive fault sites for inverter b) Resistive fault sites for NAND gate c) Resistive fault sites for NOR gate**

## III. Simulation Results

In the simulations performed in HSPICE for the basic gates a resistor is used at each fault site; the input vectors are provided and the value of the output is checked for a delay greater than 1ns. The value of the resistance is then increased at a given fault site until the delay reaches a value of 1nsec; then at same fault site, different inputs are provided. Table 1 shows the least (minimum) detectable resistance value for all fault sites of a 2 input NAND gate (the labels 1 to 15 identify the fault sites as shown in figure 1b).

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **00-11** | 800 | 825 | | | | 3500 | 3800 | 12000 | | | 220 | 150 | 130 | | 310 |
| **01-11** | 800 | | | | | 5300 | 6100 | | | | 230 | 160 | 160 | | 340 |
| **10-11** | | 800 | | | | | | 9000 | | | 230 | 200 | 140 | | 340 |
| **11-00** | | | | | | | | | | | | | | 145 | 260 |
| **11-01** | 850 | | | | | | | | 150 | 220 | | | | 180 | 240 |
| **11-10** | | 850 | 2500 | 140 | 200 | | | | | | | | | 130 | 240 |

**Table 1: Least detectable resistance (kΩ) for each fault site of a 2 input NAND gate at 180nm**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **00-11** | 120 | | | | | | | | | | | | | | 320 |
| **01-00** | 140 | | | | 1400 | 650 | | | | | | | 140 | 240 | 260 |
| **10-00** | 120 | | 600 | | | | | | | | | | 160 | 230 | 260 |
| **11-00** | | | 900 | | 1200 | 550 | | | | | | | 140 | 200 | 230 |
| **00-01** | | | | | | 400 | 5200 | | 150 | 150 | | 220 | | | 280 |
| **00-10** | | | 750 | 4500 | | | | 110 | 140 | | 160 | | | | 280 |

**Table 2: least detectable resistance (kΩ) for each fault site of 2 input NOR gate at 180nm**

The leftmost column shows input vector pairs; only six of the twelve possible input vector pairs are considered as only these pairs produce transition at the output. The values in green show the least detectable resistance value for each fault site for the specified input vector. For example, the fault at site 1 of a NAND gate can be detected by the input vectors 00->11 or 01->11 if the value of the fault resistance is at least 800 kΩ. Moreover this is the only site on which a fault can be detected for both the low to high and high to low transition cases. The fault at site 1 (i.e. at the input signal A) can only be detected if there is a transition (either 0 to 1 or 1 to 0) on A and this condition is not applicable to all vectors (for example the fault at site 15 can be detected by all vectors). The value in red shows the minimum (least) detectable value for the gate, i.e. below this value none of the faults can be detected. Once all resistance values for detectable faults are found, then the value of the resistance differs *depending on the site* of the fault.

Some faults are at critical sites such as between Vdd and the PMOS (sites 4, 9 and 14 for the NAND gate and site 1 of the NOR gate) or between the NMOS and ground (site 13 for the NAND gate and sites 8,9,10 for the NOR gate). These faults are easily detectable compared to the faults located at the gates. The minimum value of resistance detectable for any fault located between Vdd and PMOS (site 14) in the NAND gate is 130 kΩ and it can be detected by the vectors 11->01 i.e. when there is a high to low transition on B, while A is kept at a constant value. It can also be seen that most of the faults are detected by the input vectors 00->11, i.e., from Table 1, the coverage is nearly 100% by just applying the vectors 00->11, 11->00 and11->01. The above process has been repeated for 90nm, 65nm, 45nm and 32 nm technologies. Table 3 reports the values of minimum detectable resistance for an inverter at 180 nm, while Table 4 reports the results at 90 nm. The values in red are the minimum (least) detectable values for an inverter. It can be seen that even though the values change as function of feature size, the site of the fault remains the same i.e. the fault pattern and site are the same for all feature sizes.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **0->1** | | | 900 | 5000 | 170 | 250 | | 300 |
| **1->0** | 150 | 2300 | 880 | 9000 | | | 230 | 250 |

**Table 3: Least detectable resistance (kΩ) of each fault site of inverter at 180 nm**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **0->1** | | | 2400 | 10,000 | 450 | 600 | | 725 |
| **1->0** | 315 | 4700 | 2000 | 18,000 | | | 470 | 525 |

**Table 4: Least detectable resistance (kΩ) of each fault site of inverter at 90 nm**

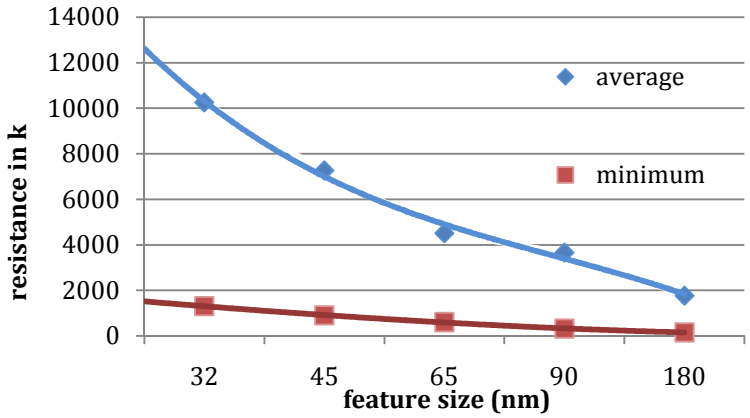


**Fig. 2: Average and minimum detectable resistance values vs. feature size for inverter**

Fig. 2 shows the effect of reducing the feature size on the average and minimum detectable resistance values for an inverter. It can be seen that as the feature size decreases the value of minimum detectable resistance increases. Similar HSPICE simulations were run for the NAND and NOR gates with the fault sites shown in Fig. 1.b) and 1.c). The results are plotted as shown in Fig. 3 for both NAND and NOR gates; the same trends as for the inverter are found.

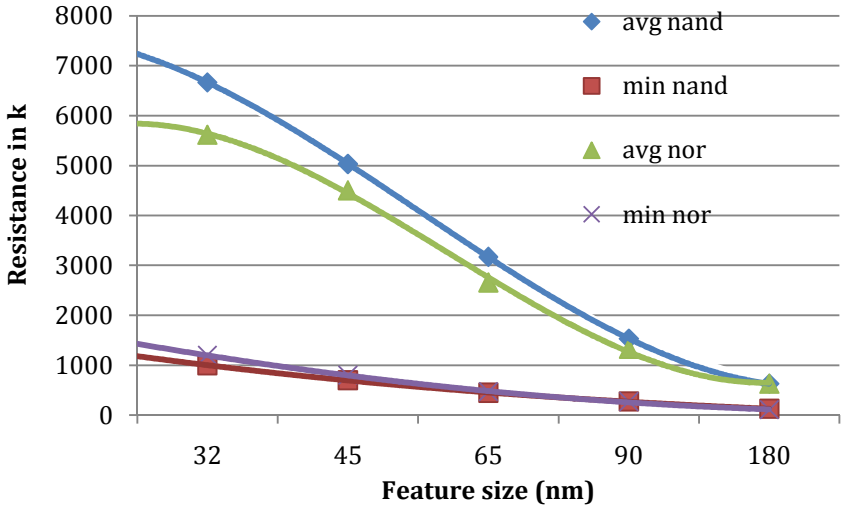


**Fig. 3: Average and minimum detectable resistance values vs feature size for NAND and NOR gates**

## IV. LOW VOLTAGE TESTING

In low voltage testing a supply voltage lower than the normal operating voltage is applied, such that the resistive open defects can be detected at a lower value of resistance [15]. As the supply voltage Vdd decreases, the drain current also decreases with however an increase in delay. For low voltage testing Vdd values 20% below the original value are considered. Simulations have been performed for four different values of voltage supply below the original value of each technology scaling. For example at 180 nm, the original supply of 1.5V is reduced by 20% i.e. till 1.2V. Five different simulation runs have been performed with variable voltages between 1.5V to 1.2V. It is found that as the supply voltage is reduced, the value of the average detectable resistance decreases. At 1.2V the defect resistance can be detected at a much lower value than the value of the resistance at 1.5V. Fault detection remains the same even at a lower voltage i.e. the values of the minimum and maximum resistance are at the *same* site for all *voltage values* and *feature sizes*.

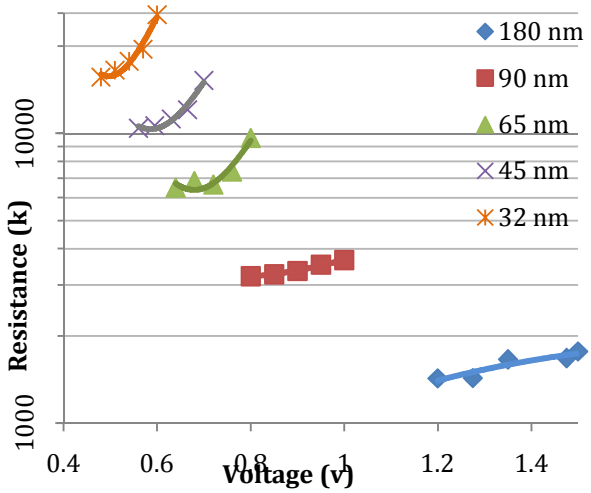


**Fig. 4: Average detectable resistance values vs low voltage for inverter testing**

As shown in Fig. 4 as the feature size decreases the effect of lowering the voltage increases; the percentage decrease is more pronounced at lower feature sizes because at nanoscaled feature sizes, the fault can be detected at a lower value for the same percentage of voltage decrease. Simulation for low voltage testing has also been performed for the 2-input NAND and NOR gates. The voltage values decrease by the same difference as for the inverter. Unlike the inverter, the average value of the resistance does not decrease with the decrease in supply voltage (while the average value keeps on increasing with a decrease in supply voltage). The simulation results for these gates are plotted in Fig. 5 a) and Fig. 5 b); while different from the inverter, the trend is similar for both the NAND and the NOR gates.

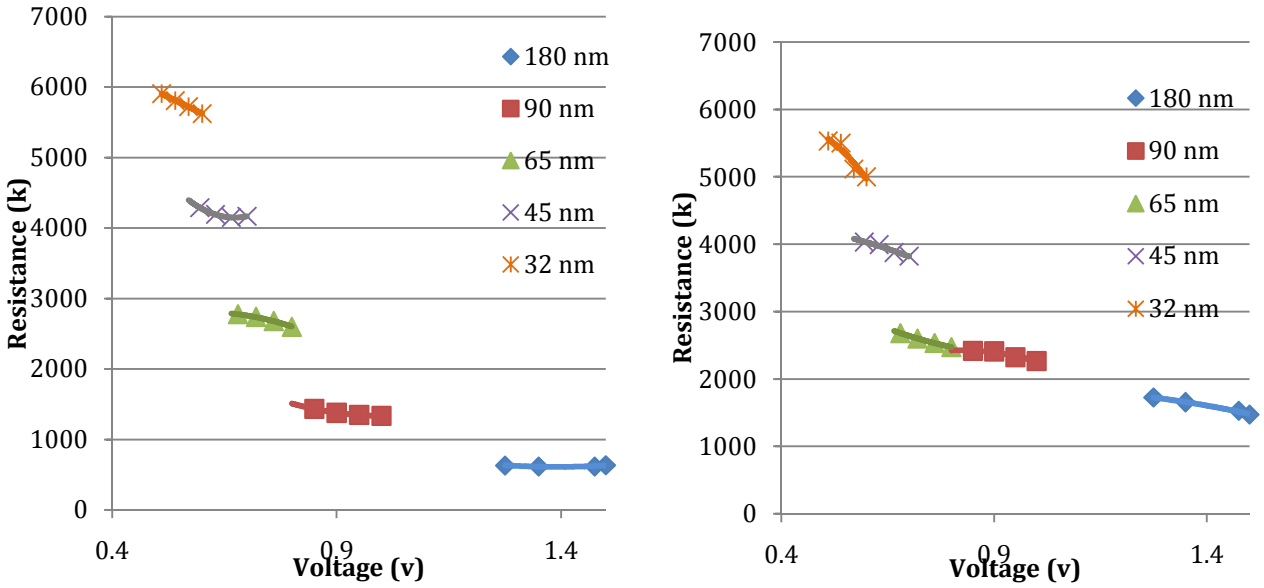


**Fig. 5: Average detectable resistance values for low voltage testing of a) NOR; b) NAND gate**

The values of the detectable resistances for both 2 input NAND and 2 input NOR gate decrease at the critical fault site, but all other values (other than at the critical sites) increase, hence the average resistance value increases too. This occurs because for some faults the reduction in the supply voltage causes also a reduction in the delay (due to the fault and the transistor itself [16]). When the former reduction in delay is less than the

increase of the latter, then the overall delay increases. This results in an increase of the overall detectable resistance value.

## V. Analytical Models

In this section, an analytical model for estimating the minimum detectable resistance is proposed. Consider the traditional expression for delay (Model 1) as

$$t_p = 0.69 \times R_{total} \times C \quad (1)$$

where $R_{total}$ is the sum of on-resistance $R_{on}$ (corresponding on the on resistance of the NMOS or PMOS depending on the fault) and the faulty resistance $R_f$ and C is the load capacitance of the inverter (Fig. 6). (1) is used to calculate the expected value of $R_{total}$ resulting in a delay $t_p$ to exceed 1 ns for both the rising and falling edges. The resistance $R_f$ can therefore be evaluated as:

$$R_f = \frac{1\ ns}{0.69 \times C} - R_{on} \quad (2)$$

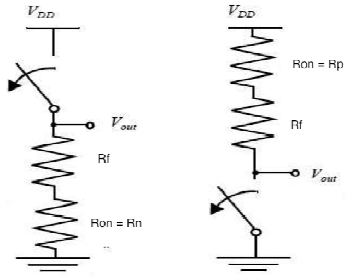


**Fig. 6: Model for fault resistance $R_f$ and $R_{on}$ for PMOS and NMOS**

The resistance values for all fault sites of an inverter are then determined and compared to the values calculated by using (2). These values for all feature sizes are plotted in Fig. 7.a) for fault site 7 and in Fig. 7 b) for fault site 1; the difference between resistance values is not negligible and increases as the feature size decreases.

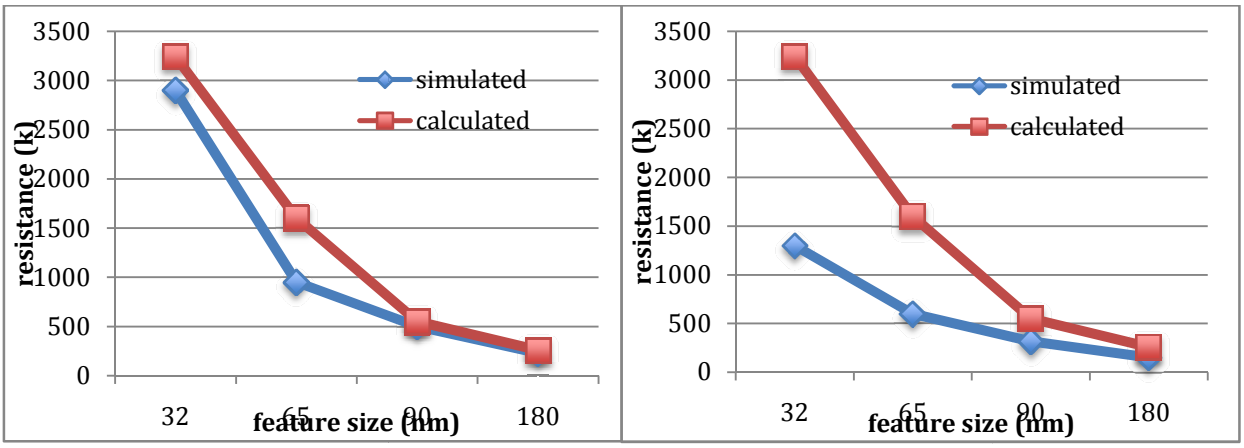


**Fig. 7: Minimum detectable resistance vs feature size for inverter at fault sites 7 (a) and 1 (b) (Model 1)**

To reduce the error, the contribution of the *gate current* is added to (2) (Model 2). The following formulas are therefore used to calculate the least resistance detectable values.

$$Rp = \frac{(Vout - Vdd)}{I} \quad (3)$$

$$Rn = \frac{Vout}{I} \quad (4)$$

$$I = I_d + I_g \quad (5)$$

In (3), the total current (I) is given by the sum of the gate current $I_g$ and the drain current $I_d$. The errors (in percentages) found using (3) is significantly less than by using Model 1; the values of the percentage error in the detectable resistance before and after the addition the of gate current are shown in Fig. 8, i.e. after adding the gate current, the error values decrease for the inverter (Fig. 8.a)), the NOR (Fig. 8.b) and the NAND gates (Fig. 8.c).

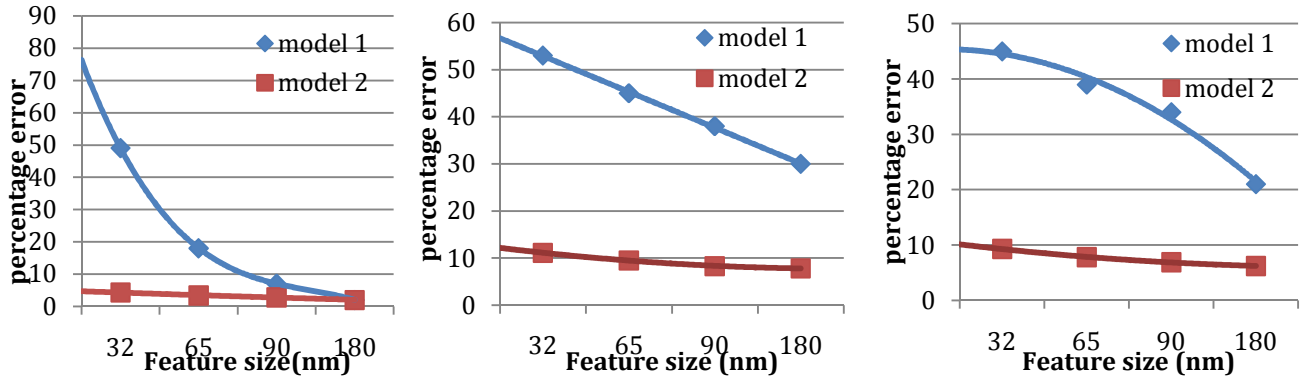


**Fig 8: Error in resistance value for both models for a) INV b) NOR c) NAND**

## VI. CONCLUSION

A detailed study of the effects of a resistive open defect on CMOS gates has been presented. The critical fault sites that produce a 1 nanosecond delay at the least (minimum) value of resistance have been identified for the inverter, NAND and NOR gates. The critical fault site is the same for all feature sizes of any particular gate. Low voltage testing of the nanoscaled CMOS gates has also been investigated to detect faults at lower resistance values; it has been found that detection of a fault can be achieved with a small decrease in the supply voltage. The low voltage test has been simulated for different feature sizes and it has been found that it can detect faults at lower values of nanoscaled feature size and hence, it is not technology dependent. For the gates, the value of the average detectable resistance increases with a decrease in voltage, but the resistance at some of the critical fault sites decreases when the supply voltage is changed. Finally, an analytical model to evaluate the minimum detectable resistance is proposed and his accuracy has been compared with the results obtained by simulation.

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