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Modeling Open Defects in Nanometric Scale CMOS

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Abstract

Open defects are extremely common in CMOS circuits. They can either be a partial or complete breaking of an input line. The complete breaking of the line is referred to as strong or full open defect. Until few years ago, a full open defect on any interconnecting line has been considered as floating. In nanometric CMOS technology, in which gate leakage currents are not negligible, full open defect lines cannot be considered to be electrically isolated. The final value of the node is independent of the initial state of the node and totally depends on the topological characteristics of the gate. Experimental evidence of the behavior of all basic gates at 90nm, 64nm and 32nm is provided; this shows a decrease in the drain current to gate leakage current ratio, in the technology scaling. The effect of full opens at the gates has also been tested by varying the PVT conditions. These variations provide a range of variation for the full open input voltage and gate leakage current. The effect of full opens on various circuits like the full adder has also been documented at various nanometric levels.

1. Introduction

Open defects are present in almost all CMOS circuits in both interconnecting and logical structures [1]. A partial or total breaking of an interconnecting line is referred to as an open defect [2]. When a line breaks completely between the two end points, then this type of defect is generally known as full open. For a technology below the 90nm level, the frequency of occurrence of these defects is likely to increase; as the gate oxide thickness is of the order of 20Å or even less, due to tunneling, a gate leakage current will flow in the circuit. Over the last decades, research has been devoted to the characterization of integrated CMOS circuits in the presence of resistive and full open defects [3]. For nanometric CMOS technology, the gate oxide thickness may be scaled below 20Å and, besides the benefits of a high drive current and a low Drain-Induced Barrier Lowering (DIBL) effect, a significant gate leakage current due to direct tunneling mechanisms appears [4]. The impact of such non-negligible gate leakage currents on the behavior of floating lines has been addressed in [2]. It is known that, for negligible gate leakage technologies, the electrical behavior of full open defects in interconnects depends on the parasitic capacitance and the trapped charge on the floating structure. Below 180 nm, the gate leakage current should be also taken into consideration [5]. The analysis of defective behavior caused by gate leakage currents in circuits with open defects has been performed at 0.18um [2]. This work extends this analysis to all basic logic gates and also to the 90nm, 64nm and 32nm technology nodes. A trend in performance for further reduction in technology scaling is also provided.

Simulations have been conducted using the Predictive Technology Model (PTM) for different feature sizes [6]. A parasitic capacitance of 2fF has been used at the floating net; his parasitic capacitance has been kept

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constant to keep the same simulating conditions for different nanometer CMOS technologies [2] under the worst case conditions. The supply voltages for 90nm, 64nm and 32nm feature sizes are given by 1V, 0.8V and 0.6 V respectively.
The paper is organized as follows: in section 2, the fundamentals of tunneling leakage are provided. In section 3, a comprehensive simulation-based assessment of basic logic gates with full opens is provided for 90, 64 and 32 nm technology nodes. In Section 4 the analysis is pursued by varying process, temperature and voltage, while in section 5, full opens are introduced in various combinational circuits and their effects are analyzed. Finally in section 6 the conclusion is drawn.

2. Steady State Conditions for Open Fault

The shrinking of feature size in present CMOS technology has led to an important change in the leakage components of CMOS transistors [1]; such devices show gate leakage current through the gate oxide due to direct tunneling mechanisms; this is expected to become a significant component of the static power consumption of nanometric CMOS transistors. We assume a simple inverter to study the effect of a full open defect at the input node for 90 nm, 64 nm and 32 nm feature sizes. The full open defect is generated by disconnecting the input node from the driver. The tunneling leakage current causes the floating node to evolve from its initial to a final state. The final state of the defective node does not depend on its initial voltage. Irrespective of whether the input is 0 or VDD, the value of the final quiescent state remains the same for the floating node. Once this defective circuit reaches the steady state, the logic response of a circuit is determined by the quiescent voltage at the floating node.

As discussed in [2] the condition that determines the final quiescent state is derived from the condition that the sum of all current components flowing into and out of the floating node must be equal to zero. The condition of $I_{Gp}+I_{Gn} = 0$ yields to a set of pairs (V_{in},V_{out}) which forms a level curve; the intersection point of this curve with the transfer curve of the inverter provides the final quiescent state at the output of the defective inverter. Figure 1 shown the different current paths for an inverter with a full open defect.

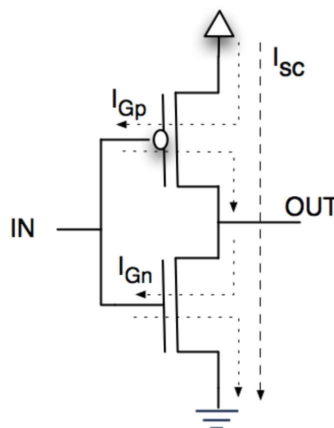

Figure 1: CMOS Inverter with input signal floating due to a full open (affecting the gate voltage of both transistors)

Simulation results show that the full open input in an inverter at 90nm remains at about 412mV, which is logic low, irrespective of the input value. The same scenario exists for 64 and 32nm technologies, with output levels of 338mV and 236mV respectively.
Differently from non nanometric technology, the presence of significant leakage currents allows to assume that the output level of an inverter with a full open defect at its inputs is not dependent from traditional parameters such as parasitic capacitance with neighboring gates, temperature, voltage and process. To validate this

assumption a Monte Carlo PVT (Process, Voltage, Temperature) analysis was performed on the inverter (Table 1). The Monte Carlo simulation involves a 3 σ variation of +/- 5% of each of the PVT parameters (process, voltage and temperature).

Table 1: Full Open Defect for an Inverter, PVT Variations

	Process Variation		Voltage Variation		Temperature Variation	
	Mean (Vin/Vdd)	Standard Deviation (σ/Vdd)	Mean (Vin/Vdd)	Standard Deviation (σ/Vdd)	Mean (Vin/Vdd)	Standard Deviation (σ/Vdd)
90nm	0.4118	**0.31%**	0.4119	**0.55%**	0.41194	**0.018%**
64nm	0.423	**0,47%**	0.4234	**0.62%**	0.4229	**0.0061%**
32nm	0,3943	**0,79%**	0.39417	**0.68%**	0.3937	**0.0055%**

3. Full Open Defect in Basic Gates

In this section, full open defects are introduced to every input of NAND and NOR 2-input gates. The results have also been taken for every combination of inputs available for the gates. The value of a full open input remains approximately constant irrespective of which input the open is located at, and the input combination. Hence, a change in the logic of the output of the gate with a full open defect is present only some combinations of the inputs; these combinations depend on the logical function of the gate.

The full open input quiescent state is independent of its initial value and reaches its final state depending on the value of the other inputs of the gate. The final quiescent state also differs with the input in which the full open defect is located, as each input in the complementary static CMOS logic has a different connection. As technology shrinks, the logic is not affected although the output comes closer to the switching threshold, thus causing the logic to possibly change. This takes place due to the increasing effect of the leakage current with respect to the drain current; the simulation results for all full open defects in NAND and NOR gates (2-inputs) are presented next for 90 nm, 64nm, and 32nm feature sizes.

3.1 NAND

The notation 2A NAND means that a full open defect has been injected at the first (or A) input of this gate; similarly, 2B NAND means that a full open defect has been injected at the second (or B) input. This notation has been used throughout the paper to establish the difference in results due to the different location of the defect in the gate. Transistors at the A input are directly connected to ground (such as in the basic inverter). Hence a slight difference in values is expected for the different full open defects. A similar notation (2A and 2B NOR) has been used for the NOR gates.

Table 2: Full Open Defect for a 2-input NAND

Technology	Logical A	Logical B	Logical output	full open input A(V)	output for full open A(V)	full open input B(V)	output for full open input B(V)	Logical full open output
90 nm	0	0	1	677.37m	1	192m	1	1
	0	1	1	399.94m	819.5m	192m	1	1
	1	0	1	677.37m	1	317m	972m	1
	1	1	**0**	399.94m	**819.5m**	317m	**972m**	**1**
64 nm	0	0	1	589.5m	800m	158m	800m	1
	0	1	1	324.3m	651m	158m	800m	1
	1	0	1	589.5m	800m	258m	786m	1
	1	1	**0**	324.3m	**651.54m**	267m	**786m**	**1**
32 nm	0	0	1	441m	600m	120m	600m	1
	0	1	1	224m	453m	120m	600m	1
	1	0	1	441m	600m	190m	583m	1
	1	1	**0**	224m	**453m**	190m	**583m**	**1**

In Table 2, the simulation results for the 2 inputs NAND gate are presented. Both for the 2A and 2B NANDs the output remains in a range for logic 1, also when the expected logic value is 0. Therefore in this case, the behavior of the NAND gate is similar to a stuck-at-1 at the output of the NAND gate.

3.2 NOR

For a NOR gate, the output goes high only when both inputs are logically low. Hence, when one input is high, the output is low irrespective of whether a full open defect is present or not at the other input. However when the other input is low and the input with the defect is supposed to be high, then the output logic switches to high (even though it should be low). For a 2 input NOR gate, the output in the presence of a full open defect is the inversion of the other input. Table 3 shows the simulation results when one of the two inputs is affected by a full open defect.

Table 3: Full Open Defect for a 2-input NOR

Technology	Logical A	Logical B	Logical ouput	full open input A(V)	output for full open A(V)	full open input B(V)	output for full open input B(V)	Logical output full open on A	Logical output full open on B
90 nm	0	0	1	426m	907m	423m	900m	1	1
	0	1	0	269m	0	423m	**904m**	0	**1**
	1	0	0	426m	**907m**	0	0	**1**	0
	1	1	0	269m	0	0	0	0	0
64 nm	0	0	1	354m	714m	351m	710m	1	1
	0	1	0	229m	0	351m	**710m**	0	**1**
	1	0	0	354m	**714m**	3.6m	0	**1**	0
	1	1	0	229m	0	3.6m	0	0	0
32 nm	0	0	1	251m	500m	250m	500m	1	1
	0	1	0	179m	0	250m	**500m**	0	**1**
	1	0	0	251m	**500m**	9.5m	0	**1**	0
	1	1	0	179m	0	9.5m	0	0	0

Both for the 2A and 2B NOR gates, the full open input remains in the range of a logic 0, corresponding to an output value that is nearly 1 when the other input is 0 (or 0 when the other input is 1). Therefore, the behavior of the NOR gate is similar to a stuck-at-0 at the input of the NOR gate.

4. PVT Variations in Logic Gates

Full open defects cause erroneous outputs for only some input combinations. The effect of a full open defect can be observed below 180nm feature size into the nanometric ranges. For basic gates depending on the output values of the inputs, the presence of a full open defect can be located; for example in an inverter, if the output is always high, then this means that a full open defect may have occurred. For a NAND gate, the full open defect can be also detected if the output is always high for any input combination; for a 2 inputs NOR gate, if the output behaves as inverting a particular input, then the full open defect can be present at the other input.

It is well known that the drain current to gate current ratio decreases with a decrease in technology feature size; this in turn will affect the value of the final quiescent state of the full open input voltage and produce an error at the output. Hence, this effect that was not observed up to 240 nm feature size, is introduced at 90 nm and lower values of feature size as shown in Figure 2.

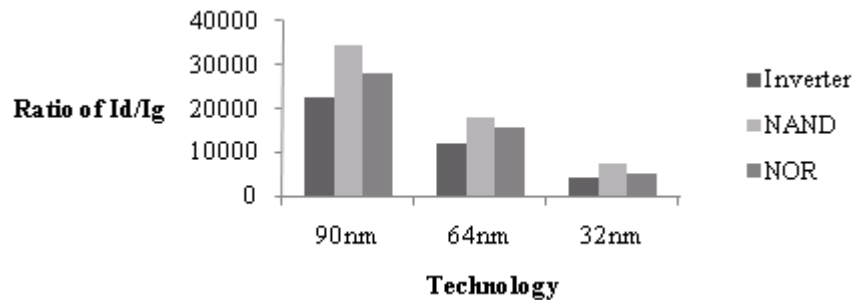

Figure 2: Id/Ig ratio vs technology feature size for different basic gates

This trend justifies the change in the behavior of open defects with respect to a non nanometric technology. The relative gate current increase creates a conductive path between the gate of the transistor affected by the open and the ground/Vdd lines of the circuits, thus fixing the voltage value of the gate independently from the initial voltage conditions.

Table 4: Process Variation, Full Open Voltage

	2 input NAND		2 input NOR	
	Mean (Vin/Vdd)	**Standard Deviation (mV)**	**Mean (Vin/Vdd)**	**Standard Deviation (mV)**
90nm	0.400	**3.09**	0.427	**1.8**
64nm	0.406	**3.435**	0.444	**2.74**
32nm	0.735	**3.65**	0.420	**3.49**

Table 4 shows the effect of process variation on the full open voltage for the NOR and NAND gates at different nanometer CMOS technologies. The mean values mostly increases as the feature size (and the supply voltage) decreases; the interesting aspect is the variation of the standard deviation with respect to feature size, i.e. the effect of process variation produces a larger change in voltage as the feature size is reduced.

It is well known that process variations affect the threshold voltage and the resistance of a gate. For nanometric CMOS technology, the effects on the threshold voltage, sheet resistance and internal capacitances are more pronounced as they are reduced; moreover, the gate leakage current and in turn, the full open input voltage that depend on these parameters, vary more and therefore, the standard deviation increases.

Table 5: Temperature Variation, Full Open Voltage

	2 input NAND		2 input NOR	
	Mean (Vin)	**Standard Deviation (mV)**	**Mean (Vin)**	**Standard Deviation (mV)**
90nm	399.94	**0.085**	426.41	**0.069**
64nm	324.31	**0.056**	354.48	**0.044**
32nm	224.06	**0.045**	251.34	**0.0244**

The temperature variation (Table 5) produces a decrease in the standard deviation as feature size is decreased; a possible reason is that the variation in the value of full open input is less that possibly a larger range of temperature variations is required. These results show that technology scales down, the effects of temperature variation on the full open input voltage will decrease.

Table 6: Voltage Variation, Full Open Voltage

	2 input NAND		2 input NOR	
	Mean (Vin)	**Standard Deviation (mV)**	**Mean (Vin)**	**Standard Deviation (mV)**
90nm	400.3	**5.11**	427	**5.29**
64nm	324.8	**4.59**	354.9	**5.03**
32nm	224.3	**3.827**	251.4	**3.93**

The full open input voltage shows a similar behavior to voltage variation as for temperature variation (Table 6). The standard deviation decreases but the ratio of mean to standard deviation increases with a decrease in feature size, thus showing that actually the effect of deviation is more predominant at smaller scaling.

5. Full Open Defects in Combinatorial Logic Circuits

For basic logic gates shown above, the presence of a full open defect has been briefly considered previously; the task of identifying the effects of a full open defect in combinational circuits is more complicated. In these circuits, the presence of a full open defect can be identified by changing every input to logical low and high and a change in output values should be observed for detection. The effects of a full open defect are then simulated next.

5.1 1 bit full adder

A 1 bit full adder has three inputs A, B and C_{in} and generates as output signals S and C_{out}. The sum S is obtained by XOR of all inputs and C_{out} is obtained by a logic circuitry using XOR, AND & OR gates. In this paper, full open defects are injected at selected inputs, i.e. a full open defect at input A (it should have 0 logic value) with the other input B=0 and C_{in}=1 (in the defect-free case, the sum is high and the C_{out} is low). However in the presence of a full open at input A, the switching threshold is exceeded, thus producing a high input at A. This causes the logic values to switch, i.e. S is low and C_{out} is high.

At 90nm, the value of the full open input just goes beyond the switching threshold, but this phenomenon is significantly more dominant at 64nm and 32nm. Similarly, for the same input values, when the full open defect is present at C_{in} , the output sum and carry are 0. Hence, the sum output switches as all inputs are logically 0. The simulation results are given in Tables 7 and 8 for all of the previously presented cases, i.e. the inputs are A=0, B=0 and C_{in}=1 (the corresponding input varied when the full open is introduced at that input).

Table 7: Full Open Defect at Input A

	Without full open defect			With full open A		
	input A	output Sum	output Carry	input A	output Sum	output Carry
90nm	1	0	1	508m	0	1
	0	1	0	**508m**	**0**	**1**
64nm	800m	0	800m	423m	0	800m
	0	800m	0	**423m**	**0**	**800m**
32nm	600m	0	600m	324m	0	600m
	0	600m	0	**324m**	**0**	**600m**

Table 8: Full Open Defect at Input Cin

	Without full open defect			With full open Cin		
	input Cin	output Sum	output Carry	input Cin	output Sum	output Carry
90nm	1	1	0	**421m**	**0**	**0**
	0	0	0	421m	0	0
64nm	**800m**	**800m**	**0**	**342m**	**0**	**0**
	0	0	0	342m	0	0
32nm	600m	600m	0	**252m**	**0**	**0**
	0	0	0	252m	0	0

5.2 Ripple Carry Adder

The ripple carry adder assumed in this study consists of three 1-bit full adders. Each full adder generates sum and carry as outputs, resulting in three sum and carry bits at the outputs of the circuit. The first full adder has two input bits designated as a0, b0 (and so on for the other cascaded adders). The first scenario consists of the three A input bits been kept high, while the B input bits are kept low. The full open is injected at b0, i.e. the B input of the first adder. This full open does not generate any change at the output because both the full open input and the input provided are at 0. The simulation results are reported in Table 9. A second scenario arises when input a2 is kept open, such that there is no change at the output. The simulation results are shown in Table 10. In this case all A inputs are 1, B inputs are 0 and C_{in}=0.

Table 9: Full Open Defect at Input b0

	Without full open defect			With full open b0		
	input b0	sum bits	carry bits output	input b0	sum bits	carry bits output
90nm	1	0	1	**303m**	**1**	**0**
	0	1	0	303m	1	0
64nm	800m	0	800m	**247m**	**800m**	**0**
	0	800m	0	247m	800m	0
32nm	600m	0	600m	**185m**	**600m**	**0**
	0	600m	0	185m	600m	0

Table 10: Full Open Defect at Input a2

	Without full open defect					With full open a2				
	input a2	output sum s3	output carry c3	other sum bits	other carry bits output	input a2	output sum s3	output carry c3	other sum bits	other carry bits output
90nm	**0**	**0**	**0**	**1**	**0**	**508m**	**1**	0	1	**0**
	1	1	0	1	0	508m	1	0	1	0
64nm	0	0	0	800m	0	**420m**	**800m**	0	800m	0
	800m	800m	0	800m	0	420m	800m	0	800m	0
32nm	0	0	0	600m	0	**324m**	**600m**	0	600m	0
	600m	600m	0	600m	0	324m	600m	0	600m	0

5.3 Carry Look ahead Generator

The 74182 is a circuit for a 4 bit carry look ahead generator. It has 4 "propagate and generate" signals obtained from the 4 primary inputs to calculate the carry of the next three bits C_{nx}, C_{ny} and C_{nz}. The other two output bits are the "propagate and generate" signals for cascading to another block. The input "propagate and generate" signals are calculated from the inputs to the circuit [7]. Full open defects are injected at P3, one of the propagate inputs and C_{ninv} (obtained by inversion of the input carry), that is always kept at 0 for this circuit to function. Hence C_{ninv} is always 1. Following input P3 as 1 and C_n as 0, all other inputs are 0 too: this would result in all outputs to be. A full open at C_{ninv} does not produce any change at the output as a full open at C_{ninv} also produces a logically 1 value. However, a full open at P3 means its value becomes 0 that would result in $\overline{P}$ and $\overline{G}$ going low at the output. This would not be the case if P3 had been logical low in the first place. This result is found at almost all nanometric feature sizes (as shown Table 11).

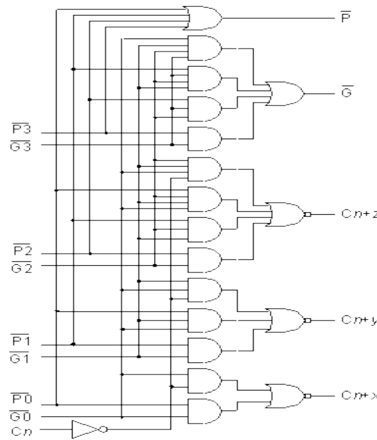

Figure 3: 74182 Gate-Level Schematic Diagram

Table 11: Full open at Input A

	Without full open defect				With full open at P3			
	input P3	$\overline{P}$	$\overline{G}$	output carries	input P3	$\overline{P}$	$\overline{G}$	output carries
90nm	1	1	1	1	432m	**0**	**0**	1
	0	0	0	1	**432m**	0	0	1
64nm	800m	800m	800m	800m	352m	0	0	800m
	0	800m	0	800m	**352m**	**0**	0	800m
32nm	600m	600m	600m	600m	255m	0	0	600m
	0	600m	0	600m	**255m**	**0**	0	600m

6. Conclusion

This paper has presented a characterization of the effect of open defects on nanoscale CMOS gates and circuits. The occurrence of open defects is very common in CMOS, therefore it is desirable to assess their presence on the gate/circuit operation. At micrometric CMOS, the presence of open faults induces a sequential behavior in a gate therefore making it necessary to use two pattern tests. In nanoscale CMOS technology however, gate leakage current is not negligible, hence full open defects on lines cannot be considered to be electrically isolated. Therefore the final value of the node is independent of the initial state and attains to a constant steady state that can be modeled as a stuck-at (and thus requiring only one test vector for detection). The effects of full opens at basic gates have also been assessed under PVT variations, showing a low impact of on the attained steady state. Finally the modeled stuck-at behavior has been applied to some logic circuits and results have been analyzed, confirming the same conclusions as for gates.

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